REMARKS

In the last Office Action, the Examiner objected to the specification as containing informalities. Claims 1-8 were rejected under 35 U.S.C. §112, second paragraph, for indefiniteness. Claims 1-8 were further rejected under 35 U.S.C. §103(a) as being unpatentable over applicants' prior art disclosure in Fig. 2 ("APD") in view of U.S. Patent No. 6,653,999 to Motegi et al. ("Motegi"). Additional art was cited of interest.

In accordance with the present response, the specification has been suitably revised to correct informalities, including those noted by the Examiner, to provide antecedent basis for the claim language, and to bring it into better conformance with U.S. practice. Original independent claims 1, 2 and 4 have been amended to further patentably distinguish from the prior art of record. Original claims 1, 2, 4, 5, 7 and 8 have also been amended to overcome the rejection under 35 U.S.C. §112, second paragraph, in formal respects to improve the wording, and to bring them into better conformance with U.S. practice. Claims 3 and 6 have been canceled without prejudice or admission, thereby rendering the rejection of these claims under 35 U.S.C. §112, second paragraph, moot. New claims 9-12 have been added to provide a fuller scope of coverage. The title of the

invention has been changed to "SWITCHED CAPACITOR AMPLIFIER CIRCUIT AND ELECTRONIC DEVICE EQUIPPED WITH SWITCHED CAPACITOR AMPLIFIER CIRCUIT", to more clearly reflect the invention to which the amended and new claims are directed. A new, more descriptive abstract has been substituted for the original abstract.

In view of the foregoing, applicants respectfully submit that the objection to the specification and the rejection of claims 1, 2, 4, 5, 7 and 8 under 35 U.S.C. §112, second paragraph, have been overcome and should be withdrawn.

Applicants request reconsideration of their application in light of the following discussion.

Brief Summary of the Invention

The present invention is directed to a switched capacitor amplifier circuit and to an electronic device equipped with the switched capacitor amplifier circuit.

Fig. 2 shows a conventional switched capacitor amplifier circuit. As described in the specification (pgs. 1-3), the conventional switched capacitor amplifier circuit has been ineffective in canceling noise components of a reference voltage during adjustment of an offset voltage between input terminals.

The present invention overcomes the drawbacks of the conventional art. Fig. 1 shows an embodiment of a switched capacitor amplifier circuit according to the present invention embodied in amended independent claim 1. The switched capacitor amplifier circuit has a pair of input terminals 141, 142, an output terminal 151, a pair of capacitors 101, 102 connected to respective input terminals 141, 142, and a pair of switch circuits 123, 124 connected to respective capacitors 101, 102 and input terminals 141, 142. Each of a pair of reference voltage terminals 111, 112 receives a reference voltage for supplying electric charges to a respective one of the capacitors 101, 102. The reference voltage terminals 111, 112 are connected to respective switch circuits 123, 124 so that noise components of the reference voltages are in phase to reduce noise during adjustment of an offset voltage between the input terminals 141, 142. By this construction, noise generated during adjustment of the offset voltage between the input terminals is effectively reduced, thereby allowing for enhanced amplification of a signal output from the output terminal 151.

In another embodiment embodied in amended independent claim 2, a switched capacitor amplifier circuit has a first input terminal 141 for receiving a first input signal, a second input terminal 142 for receiving a second

input signal, a first capacitor 101 for receiving a signal corresponding to an output of the first input terminal 141, and a second capacitor 103 for receiving a signal corresponding to an output of the second input terminal 142. An operational amplifier for compares a signal corresponding to an output of the first capacitor 101 with a signal corresponding to an output of the second capacitor 103. A first reference voltage terminal 111 receives a first reference voltage that supplies electric charges to the first capacitor 101. A second reference voltage terminal 112 receives a second reference voltage that supplies electric charges to the second capacitor 103. A control circuit (e.g., reference voltage generator) adjusts at least one of the first reference voltage and the second reference voltage so that a voltage difference between the first reference voltage and the second reference voltage coincides in phase with an offset voltage between the first input terminal 141 and the second input terminal 142.

By the foregoing construction, since the voltage difference between the first reference voltage and the second reference voltage coincides in phase with an offset voltage between the first and second input terminals, the amplification of noise is effectively eliminated during operation of the switched capacitor amplifier circuit.

Traversal of Prior Art Rejection

Claims 1, 2, 4, 5, 7 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over APD in view of Motegi. Applicants respectfully traverse this rejection and submit that the combined teachings of APD and Motegi do not disclose or suggest the subject matter recited in amended claims 1, 2, 4, 5, 7 and 8.

Amended independent claim 1 is directed to a switched capacitor amplifier circuit and requires a pair of input terminals, a pair of capacitors connected to respective input terminals, a pair of switch circuits connected to respective capacitors and input terminals, a pair of reference voltage terminals each for receiving a reference voltage for supplying electric charges to a respective one of the capacitors, the reference voltage terminals being connected to respective switch circuits so that noise components of the reference voltages are in phase to reduce noise during adjustment of an offset voltage between the input terminals. No corresponding structural and functional combination is disclosed or suggested by the prior art of record.

The primary reference to APD discloses a switched capacitor amplifier circuit as described in the specification and shown in Fig. 2. As recognized by the Examiner, APD does not disclose or suggest any circuit structure for controlling

the switch circuits and the capacitors so that noise components of a reference voltage for supplying electric charges to the capacitors are in phase to reduce noise during adjustment of an offset voltage between the input terminals, as recited in amended independent claim 1.

The secondary reference to Motegi discloses a liquid crystal driving integrated circuit. According to Motegi, liquid crystal driving voltages VLCD0-VLCD4 can be finely adjusted not only by 11 versions of reference voltage VLCD0 in accordance with voltages at respective connection points of 12 serially connected resistor elements, but by changing the resistance of an external variable resistor 25, to thereby provide a liquid crystal driving integrated circuit that can be used for a variety of general purposes (see Abstract). Thus, in a first instance, the liquid crystal driving integrated circuit disclosed by Motegi does <u>not</u> correspond either in structure or function to a switched capacitor amplifier circuit, as required by amended independent claim 1.

Second, it is unclear how the integrated circuit disclosed by Motegi generates reference voltages at two nodes (reference voltage terminals) utilizing a reference voltage generating circuit. However, even if Motegi provides such disclosure, applicants submit that Motegi does not disclose or

suggest the specific structural connection between the reference voltage terminals and switch circuits and the corresponding function recited in amended independent claim 1. More specifically, amended claim 1 requires reference voltage terminals connected to respective switch circuits, which in turn are connected to respective capacitors and input terminals, so that noise components of the reference voltages are in phase to reduce noise during adjustment of an offset voltage between the input terminals. Motegi clearly does not disclose or suggest reference voltage terminals connected to respective switch circuits, and further for the purpose of providing for noise components of the reference voltages to be in phase to reduce noise during adjustment of an offset voltage between the input terminals, as required by amended independent claim 1.

Amended independent claim 4 similarly distinguishes from the combined teachings of APD and Motegi. More specifically, with reference to the embodiment of the present invention shown in Fig. 1, amended independent claim 4 requires a single reference voltage generator for generating a first reference voltage at a first reference voltage terminal 111 connected to another end of the third switch circuit 123 (i.e., which is connected to the first capacitor 101 and to one of the input terminals of the operational amplifier) and a

second reference voltage at a second reference voltage terminal 112 connected to another end of the fifth switch circuit 124 (i.e., which is connected to the third capacitor 102 and to the other of the input terminals of the operational amplifier). It is evident that Motegi does not disclose or suggest reference voltage terminals connected to the respective switch circuits as recited in amended independent claim 4.

Amended independent claim 2 is also directed to a switched capacitor amplifier circuit and requires a first reference voltage terminal for receiving a first reference voltage that supplies electric charges to the first capacitor, a second reference voltage terminal for receiving a second reference voltage that supplies electric charges to the second capacitor, and a control circuit for adjusting at least one of the first reference voltage and the second reference voltage so that a voltage difference between the first reference voltage and the second reference voltage coincides in phase with an offset voltage between the first input terminal and the second input terminal. As recognized by the Examiner, no corresponding structure and function is disclose or suggested by APD.

Likewise, even if Motegi were interpreted to disclose the generation of reference voltages at two nodes

(reference voltage terminals) utilizing a reference voltage generating circuit, the reference clearly does not disclose or suggest any circuit structure for adjusting at least one of the reference voltage so that a voltage difference between the reference voltages coincides in phase with an offset voltage between two input terminals, as required by amended independent claim 2.

Since Motegi does not disclose or suggest the foregoing structural and functional features recited in amended independent claims 1, 2 and 4, the reference does not cure the deficiencies of APD. Accordingly, one ordinarily skilled in the art would not have been led to modify the references to attain the claimed subject matter.

Claims 5, 7 and 8 depend on and contain all of the limitations of amended independent claims 4, 2 and 1, respectively, and, therefore, distinguish from the references at least in the same manner as claims 4, 2 and 1.

In view of the foregoing, applicants respectfully request that the rejection of claims 1, 2, 4, 5, 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over APD in view of Motegi be withdrawn.

Applicants respectfully submit that the prior art of record also does not disclose or suggest the subject matter recited in newly added claims 9-12.

New independent claim 9 is directed to a switched capacitor amplifier circuit and requires an operational amplifier having a pair of input terminals, a plurality capacitors and switch circuits each connected to one of the input terminals of the operational amplifier, and a single reference voltage generator for generating first and second reference voltages at first and second reference voltage terminals, respectively, for supplying electric charges to the capacitors, the first reference voltage terminal being connected to one of the switch circuits connected to one of the input terminals of the operational amplifier and the second reference voltage terminal being connected to another of the switch circuits connected to the other of the input terminals of the operational amplifier. Claim 9 further requires a control circuit for adjusting at least one of the first reference voltage and the second reference voltage so that a voltage difference between the first reference voltage and the second reference voltage coincides in phase with an offset voltage between the input terminals of the operational amplifier. No corresponding structural and functional combination is disclosed or suggested by the prior art of record as set forth above for amended independent claims 1, 2 and 4.

Claims 10-12 depend on and contain all of the limitations of independent claim 9 and, therefore, distinguish from the prior art of record at least in the same manner as claim 9.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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February 28, 2005
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